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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,748	10/30/2003	Bruce B. Doris	FIS920030264 (00750483AA)	6189

30743 7590 11/06/2007

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ART UNIT	PAPER NUMBER
2814	

MAIL DATE	DELIVERY MODE
11/06/2007	PAPER

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/695,748
Filing Date: October 30, 2003
Appellant(s): DORIS ET AL.

Marshall M. Curtis
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 06/21/07 appealing from the Office action mailed 8/17/06.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

2003/0181005	Hachimine	09-2003

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 10-12 and 16-19 are rejected under 35 U.S.C. 102(e) as being anticipated by US Pub2003/0181005 to Hachimine et al.

Regarding claim 10, Hachimine discloses a structure that adjusts carrier mobility in CMOS transistors in fig. 24 or 31 comprising: a substrate 1 [0164], a first transistor (n-ch MISFET) having a gate dielectric 5, gate electrode 6, and source/drain 7/10 [0165], and gate region 12 [0167], formed on said substrate 1, a second transistor (p-ch MISFET) having a gate dielectric 5, gate electrode 6, and source/drain 8/11, and gate regions 12, fig. 15, formed on said substrate 1, a first film 14a providing tensile stress [0168] at least at the channel of first transistor, a second film 14b providing compressive stress [0168] at least at the channel of second transistor, a portion of said second film 14b extending in the same region of said substrate as a portion of said first film 14a, fig. 24 or 31, and a shear force isolation layer 15 [0170] separating said first film 14a and

said second film 14b and said tensile and compressive stress therein in at least one area, fig. 15.

Regarding claim 11, Hachimine discloses the structure wherein the first tensile stress and second compressive stress films can be composed of nitride, oxide [0168].

Regarding claim 12, Hachimine discloses the structure wherein the first tensile and second compressive stressed films 14a/14b are separated by said shear force isolation layer 15 at all points of overlap, fig. 24 or 31.

Regarding claim 16, Hachimine discloses the structure wherein said first and second stressed films 14a/14b are separated by the shear force isolation layer 5 at selected areas.

Regarding claim 17, Hachimine discloses the structure wherein said first stressed film 14a, closer to the substrate than said second stressed film 14b, fully surrounds the NMOS transistor, fig. 31.

Regarding claim 18, Hachimine discloses the structure wherein said first stressed film 14a is the only separation between the nMOS transistor and said second stressed film 14b, fig. 31.

Regarding claim 19, Hachimine discloses the structure wherein said second stressed film 14b surrounds said oxide liner 9 at the sides of the PMOS transistor gate electrode 6 with the top of the gate directly engaged with said second stressed film 14b, fig. 31.

Allowable Subject Matter

3. Claims 13-15 would be allowable if rewritten to overcome the rejection(s) under The prior art of record neither anticipated nor rendered obvious all the limitations of claim 13 including 'the first stressed film, closer to the substrate than the second stressed film, does not fully surround the nMOS transistor, but rather the sides only, while the remaining surfaces of the nMOS transistor are contacted by said shear force isolation layer'.

(10) Response to Argument

4. The Applicant argues essentially that the dielectric layer 120 in fig. 6 of the instant application is "shear force isolation layer", while layer 15 in fig. 31 of Hachimine does not constitute a "shear force isolation layer" as claimed. The Examiner respectfully disagrees and submits layer 15 of Hachimine is "a shear force isolation layer" for the following reasons:

a. The Appellant defines layer 120 as "a dielectric layer" in page 12 lines 5. There is no detail to further defining the dielectric layer 120 and the Appellant claims such dielectric layer as "a shear force isolation layer". The Examiner submits that the layer 15 of Hachimine is an insulating (dielectric) layer [0196]; therefore it can equivalently call as or function as "a shear force isolation layer", see MPEP 2112.01.

b. In the Appellant final structure in fig. 6, layer 120 is interposed between a bottom tensile stress layer 11 and a top compressive stress layer 13. The interpretation of "a shear force isolation layer" is a layer in between the tensile

and compressive stress layers. The Examiner respectfully submits that as disclosed by Hachimine in fig. 31, layer 15 is interposed between a bottom tensile stress layer 14a and a top compressive stress layer 14b [0168], such structure is substantially identical to the claimed structure. Thus, layer 15 of Hachimine reads on the claim limitation as "a shear force isolation layer" because the structure recited in Hachimine is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent, see MPEP 2112.01.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Thao X. Le TL

29 Oct. 2007

Conferees:

Mr. R. Mack, SPE RM

Mr. W. Fahmy, SPE W.F